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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,627	07/17/2003	Michael Green	RA-307	2652

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,627	GREEN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6,9-19 and 21* is/are allowed.

6)☒ Claim(s) *1-3,8 and 20* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are presented in the instant application according to the Applicants' amendment filed on 09/07/2004.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3, 8 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (U.S. Pub. No. 2002/0180540).

With respect to claim 1, Hirai discloses, in Figure 1, a circuit and its corresponding method comprising the steps of a) determining [11] a cycle period of first clock signal [reference signal]; b) detecting [11] rising and falling edges of a second clock signal [feedback signal] during the cycle period the first clock signal; and c) designating the cycle period of the first clock signal as valid when a single rising edge *(Fig. 2, tNA+1)* of the second clock signal and a single falling edge *(Fig. 2, a)* of the second clock signal are detected during the cycle period of the first clock signal.

With respect to claim 2, Hirai discloses, in Figure 1, that the first clock signal is a reference clock signal and the second clock signal is a feedback clock signal.

With respect to claim 3, Hirai discloses, in Figure 1, that the determining the cycle period of the first clock signal further comprises detecting [11] a rising edge of the first clock signal and detecting [11] an immediately following rising edge the first clock signal.

With respect to claim 8, Hirai discloses, in Figure 1, that wherein the first clock signal is a reference clock signal and the second clock signal is a skewed *(skewed since having to propagate through components such as [12,13,14] along the feedback path)* feedback clock signal.

With respect to claim 20, Hirai discloses, in Figure 1 and paragraph [0062], lines 14-16, a circuit comprising phase-locked loop circuit that receives a reference clock signal and generates a feedback clock signal; and means for detecting [20] when the feedback clock signal and the reference clock signal are out of lock, wherein the means detects that the feedback clock signal and the reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period and when a single rising edge and a single falling edge of the feedback clock signal are detected during less than a predetermined number of the reference clock cycles during the time period.

Allowable Subject Matter

3. Claims 5, 6, 9-19 and 21 are allowed.

4. Claims 4 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter.

The closest prior art on record does not show or fairly suggest:

a) A method including the step of counting a number of consecutive cycle periods of first clock signal that are designated as valid, as called for in claim 4;

b) The method further including a step of comparing a predetermined full count number to the number of consecutive cycle periods of the first clock signal that are designated as valid; and asserting a lock signal when the predetermined full count number substantially equals the number of consecutive cycle periods of the first clock signal that are designated as valid, as called for in claim 5;

c) The method further including a step of comparing a predetermined full count number to the number of consecutive cycle periods of the first clock signal that are designated as valid; and asserting a lock signal when the number of consecutive cycle periods of the first clock signal that are designated as valid exceeds the predetermined full count number by two, as called for in claim 6;

d) The method, in which the step of designating the cycle period of the first clock signal as valid further comprises detecting a single rising edge of a skewed second clock signal and a single falling edge of the skewed second clock signal during a subsequent cycle period the first clock signal, as called for in claim 7;

e) A circuit including a valid counter that receives the first clock signal and signal and outputs a lock signal, the valid cycle counter counting a number of consecutive cycle periods of the first clock signal during which the valid cycle detector has asserted the valid cycle signal, the valid cycle counter asserting the lock signal when the number of consecutive cycle periods of the

first clock signal during which the valid cycle detector has asserted the valid cycle signal exceeds a predetermined number, in combination with the remaining claimed limitations, as called for in claim 9;

f) A circuit including a lock detection circuit, the lock detection circuit counting a number of rising and falling edges of the feedback clock signal during a period of the reference clock signal, the lock detection circuit generating a valid cycle signal having a first value when exactly one rising edge and exactly one falling edge is counted and having a second value when another number of rising edges and falling edges counted, in combination with the remaining claimed limitations, as called for in claim 19; and

g) A circuit including a means for outputting a lock signal when a number consecutive valid cycles of the reference clock signal exceeds a predetermined number, in combination with the remaining claimed limitations, as called for in claim 21.

Remarks

6. Applicant's arguments filed 09/07/2004 have been fully considered but they are not completely persuasive.

7. With respect to the Applicants' argument on page 8, second paragraph regarding the statement that Hirai in not prior art under the version of § 102(e) that is the basis for the rejection because Hirai is not a granted patent; Hirai qualifies for 102(e) rejection in accordance with 35 U.S.C. § 102(e) and 374 as amended by H.R. 2215.

With respect to the Applicants' argument regarding claim 1, page 8, last paragraph, the examiner disagrees with the Applicants' statement of *"Hirai does not disclose the third element recited in claim 1: "designating the cycle period of the first clock signal as valid when a single*

rising edge of the second clock signal and a single falling edge of the second clock signal are detected during the clock period of the first clock signal."". As clearly shown in Fig. 2, Hirai discloses the step of designating the cycle period of the first clock signal as valid when a single rising edge *(Fig. 2, tNA+1)* of the second clock signal and a single falling edge *(Fig. 2, a)* of the second clock signal are detected during the cycle period of the first clock signal *reference signal)*.

With respect to the Applicants' argument regarding claim 3, page 10, last paragraph, the examiner disagrees with the Applicants' statement of *"Hirai does not disclose a means for determining a cycle period between a rising edge and an immediately following rising edge"*. As clearly shown in Fig. 2, Hirai discloses the step of determining a cycle period of the first clock signal which is the reference signal between a rising edge *(first rising edge)* and an immediately following rising edge *(second rising edge)*.

With respect to the Applicants' argument regarding claim 20, page 12 bridging page 13, the examiner disagrees with the Applicants' statement of *"Hirai does not disclose all of the limitations of amended claim 20"*. As clearly shown in Fig. 2, Hirai discloses in Figure 1 and paragraph [0062], lines 14-16, a circuit comprising phase-locked loop circuit that receives a reference clock signal and generates a feedback clock signal; and means for detecting [20] when the feedback clock signal and the reference clock signal are out of lock, wherein the means detects that the feedback clock signal and the reference clock signal are out of lock when a like number of feedback clock cycles and reference clock cycles occur during a time period and when a single rising edge and a single falling edge of the feedback clock signal are detected during less than a predetermined number of the reference clock cycles during the time period.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER